Amendments to the Claims

This listing will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claim 1 (currently amended): A memory control apparatus, adapted to operate with a plurality of digital signal processors (DSPs), the memory control apparatus comprising:

a switch, adapted to selectively route signals for input to the DSPs from a memory and for output from the DSPs to the memory;

a buffer coupled to an insert terminal of the memory and of each DSP, the buffer being adapted to receive memory information comprising an insert signal from the memory and output the insert signal to the insert terminal of each DSP ~~adapted~~ to selectively output to the DSPs ~~memory~~ information indicating that the memory is available; and

a controller, adapted to control the switch to route the signals to and from the memory and DSPs and to control the buffer to selectively output the memory information.

Claim 2 (original): A memory control apparatus as claimed in claim 1, wherein:

the memory is a removable memory, and the memory information indicates that the memory has been inserted into a port for access by the memory control apparatus.

Claim 3 (original): A memory control apparatus as claimed in claim 2, wherein:

the memory is a flash memory.

Claim 4 (original): A memory control apparatus as claimed in claim 1, wherein:

the switch includes a plurality of selection switches, coupled between the DSPs and the memory, which are controlled by the controller.

Claim 5 (original): A memory control apparatus as claimed in claim 1, wherein:

the buffer includes a three-state buffer which selectively outputs the memory information of the memory to the DSPs as controlled by the controller.

Claim 6 (original): A memory control apparatus as claimed in claim 1, further comprising:

a key input unit, adapted to indicate an operation mode; and

wherein the control unit controls recording of data in the memory or reproduction of data from the memory according to the operation mode indicated by the key input unit.

Claim 7 (original): A memory control apparatus as claimed in claim 1, wherein:

one of the DSPs is employed with a digital still camera and another of the DSPs is employed with a digital video camera; and

wherein the controller controls the switch to route the signals to and from the memory and the DSPs of the digital still camera and digital video camera.

Claim 8 (currently amended): A method for controlling a memory control apparatus having a controller to operate with a plurality of digital signal processors (DSPs), the method comprising:

controlling a switch to selectively route signals for input to the DSPs from a memory and for output from the DSPs to the memory; and

controlling a buffer ~~to selectively output to the DSPs memory information indicating that the memory is available~~ to receive memory information comprising an insert signal from the memory and selectively output the insert signal to an insert terminal of each DSP, the buffer being coupled to an insert terminal of the memory and of each DSP.

Claim 9 (original): A method as claimed in claim 8, wherein:

the memory is a removable memory, and the memory information indicates that the memory has been inserted into a port for access by the memory control apparatus.

Claim 10 (original): A method as claimed in claim 9, wherein:

the memory is a flash memory.

Claim 11 (original): A method as claimed in claim 8, wherein:

the switch includes a plurality of selection switches, coupled between the DSPs and the memory; and

the switch controlling step includes controlling the plurality of switches.

Claim 12 (original): A method as claimed in claim 8, wherein:

the buffer includes a three-state buffer; and

the buffer controlling step controls the three-state buffer to selectively output the memory information of the memory to the DSPs.

Claim 13 (original): A method as claimed in claim 8, further comprising:

receiving information from a key input unit indicating an operation mode; and

controlling recording of data in the memory or reproduction of data from the memory according to the operation mode indicated by the key input unit.

Claim 14 (original): A method as claimed in claim 8, wherein:

one of the DSPs is employed with a digital still camera and another of the DSPs is employed with a digital video camera; and

wherein the switch controlling step controls the switch to route the signals to and from the memory and the DSPs of the digital still camera and digital video camera.

Claim 15 (currently amended): A computer-readable medium of instructions for controlling a memory control apparatus <u>having a controller</u> to operate with a plurality of digital signal processors (DSPs), the computer-readable medium of instructions comprising:

a first set of instructions, adapted to control a switch to selectively route signals for input to the DSPs from a memory and for output from the DSPs to the memory; and

a second set of instructions, adapted ~~to control a buffer to selectively output to the DSPs memory information indicating that the memory is available~~ <u>to receive memory information comprising an insert signal from the memory and selectively output the insert signal to an insert terminal of each DSP, the buffer being coupled to an insert terminal of the memory and of each DSP</u>.

Claim 16 (original): A computer-readable medium of instructions as claimed in claim 15, wherein:

the memory is a removable memory, and the memory information indicates that the memory has been inserted into a port for access by the memory control apparatus.

Claim 17 (original): A computer-readable medium of instructions as claimed in claim 16, wherein:

the memory is a flash memory.

Claim 18 (original): A computer-readable medium of instructions as claimed in claim 15, wherein:

the switch includes a plurality of selection switches, coupled between the DSPs and the memory; and

the first set of instructions is adapted to control the plurality of switches.

Claim 19 (original): A computer-readable medium of instructions as claimed in claim 15, wherein:

the buffer includes a three-state buffer; and

the second set of instructions is adapted to control the three-state buffer to selectively output the memory information of the memory to the DSPs.

Claim 20 (original): A computer-readable medium of instructions as claimed in claim 15, further comprising:

a third set of instructions, adapted to control the memory control apparatus to receive information from a key input unit indicating an operation mode; and

a fourth set of instructions, adapted to control the memory control apparatus to control recording of data in the memory or reproduction of data from the memory according to the operation mode indicated by the key input unit.

Claim 21 (original): A computer-readable medium of instructions as claimed in claim 15, wherein:

one of the DSPs is employed with a digital still camera and another of the DSPs is employed with a digital video camera; and

wherein the first set of instructions controls the switch to route the signals to and from the memory and the DSPs of the digital still camera and digital video camera.